REMARKS

The Applicant thanks the Examiner for the careful examination of this application and respectfully requests the entry of the amendments indicated hereinabove. The Applicant also thanks the Examiner for the indication of allowance of claims 1-5.

Claims 1-13 and 15-19 are pending. Claims 6-13 and 15-19 are rejected.

In response to the 35 U.S.C. §112, first paragraph rejection, the Applicant respectfully traverses the statement in the Office Action that "The Specification is not enabling for the limitation because it does not mention that the bodies are not tied to any fixed potential." The Applicants submits that Claim 10 is enabled, for example, by Figures 8-9 and the corresponding description on pages 10-11.

The Applicant also respectfully traverses the statement in the Office Action that "It seems that if a source or drain is tied to a fixed potential, then the body of the transistor is also tied to a fixed potential." The Applicant submits that, while it may seem that the body may be tied to a fixed potential, in practice the body is in an area of opposite diffusion type (i.e. n-type or p-type) to the source and drain. As a result, when there is a single connection to the source or drain the entire silicon mesa tends, in the DC condition, to be at the same potential; therefore, the device would have no use (and would have no impact on the total circuit). However, when a second (different) potential is applied to the drain, the body will attain its own potential - which will vary depending on the rate of change of the voltage on the

other pins (i.e. drain, gate, and source) and the temperature (which will modify leakage). The Applicant respectfully submits that this is in no way equivalent to being tied to a fixed potential.

Claim 6 positively recited a pair of transistors in an analog circuit stage which requires matched behavior of the transistor pair. In addition, Claim 6 positively recites a physical connection of metallic material which provides thermal conduction between respective bodies of a pair of transistors. These advantageously claimed features are not taught or suggested by the patents granted to Flaker et al. or Houston et al., either alone or in combination.

The Applicant respectfully traverses the indication in the Office Action (page 8) that "In fact, metals naturally have the properties of electrical conduction and thermal conduction. Because Flaker teaches the use of metal to provide an electrical link between transistors, then Flaker inherently teaches that link provides thermal conduction." The Applicant agrees that metals have both thermal and electrical properties; however, the Applicant submits that metals in configurations having good electrical conduction don't necessarily have good thermal properties. For example, if heat dissipated strongly down metal wires, then the wires of an electric space heater would get hot through conduction from the element – which they clearly do not.

The Applicant respectfully traverses the indication in the Office Action (page 3) that Flaker et al. teaches, in column 6 line 53 through column 7 line 4, a physical connection of metallic material for a pair of transistors in an analog circuit

stage. The Applicant submits that Flaker et al. is discussing a digital application (column 6 lines 56-59, column 7 lines 3-4) that may use a metal link instead of silicon. Arguably this implies that Flaker et al. does not comprehend the use of metal links in SOI analog circuit stages.

The Applicant notes that in the application shown in FIG. 10B that Flaker et al. teaches the addition of an extra oxide layer (40) that would reduce the thermal coupling (column 5 lines 49-55); and therefore teaches away from providing thermal conduction between respective bodies of the pair of transistors as advantageously claimed.

Houston et al. does not teach a physical connection that provides thermal conduction between respective bodies of transistors as advantageously claimed. Rather, Houston et al. teaches electrical conduction between two transistors in an SRAM (column 4 lines 25-28, column 9 lines 35-42; column 17 lines 20-37). Houston et al. does not teach providing thermal conduction between respective bodies of a pair of transistors in an analog circuit stage as advantageously claimed.

Therefore, the Applicant respectfully traverses the Examiner's rejection of Claim 6 and respectfully asserts that Claim 6 is patentable over Flaker et al. and Houston et al., either alone or in combination. Furthermore, Claims 7 – 9 are allowable for depending on allowable independent Claim 6 and, in combination, including limitations not taught or described in the references of record.

Amended Claim 10 positively recites that transistor bodies are thermally coupled by a connection of non-insulating material. These advantageously claimed features are not taught or suggested by the patent granted to Houston et al.

Houston et al. does not teach a physical connection that provides thermal conduction between respective bodies of transistors as advantageously claimed. Rather, Houston et al. teaches electrical conduction between two transistors (column 9 lines 35-42; column 17 lines 20-37). The Applicant submits that configurations having good electrical conduction don't necessarily have good thermal properties. There is no reason to believe that the circuit of Houston et al.'s FIG. 5a has bodies that are thermally coupled by a connection of non-insulating material as advantageously claimed.

Therefore, the Applicant respectfully traverses the Examiner's rejection of Claim 10 and respectfully asserts that Claim 10 is patentable over Houston et al. Furthermore, Claims 11 – 13 and 15 are allowable for depending on allowable independent Claim 10 and, in combination, including limitations not taught or described in the references of record.

Claim 16 positively recites a physical connection of material which provides thermal conduction between respective bodies of a pair of transistors. These advantageously claimed features are not taught or suggested by the patent granted to Flaker et al.

The Applicant respectfully traverses the indication in the Office Action (page 8) that "In fact, metals naturally have the properties of electrical conduction and thermal conduction. Because Flaker teaches the use of metal to provide an electrical link between transistors, then Flaker inherently teaches that link provides thermal conduction." The Applicant agrees that metals have both thermal and electrical properties; however, the Applicant submits that metals in configurations having good electrical conduction don't necessarily have good thermal properties.

In addition, the Applicant submits that Flaker et al. merely teaches equilibration of the body charge differentials due to thermal effects (column 4 lines 60-67); which is entirely different than equalizing the thermal effects (i.e. is less efficiently equalized in Flaker's partial trench scheme than in a scheme that does not constrict the conductive silicon height).

The Applicant notes that if Flaker et al. had been discussing thermal connectivity then he would not have formed a more thermally resistive silicon link – which is what is being done by the addition of the extra process step that he is using to get the so called 'partial trench'.

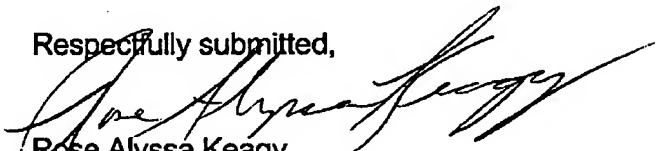
The Applicant also notes that in the application shown in FIG. 10B that Flaker et al. teaches the addition of an extra oxide layer (40) that would reduce the thermal coupling (column 5 lines 49-55); and therefore teaches away from providing thermal conduction between respective bodies of the pair of transistors as advantageously claimed.

The Applicant respectfully traverses the indication in the Office Action (page 4) that Flaker et al. teaches a body link (32) that does not carry current during normal operation of the circuit. The Applicant submits that Flaker et al.'s intrinsic silicon bridge (despite a high resistance) will still conduct electricity (though it may indeed be a poor conductor compared to highly doped silicon). Flaker et al. even states that an electrically conductive bridge is formed (column 5 lines 1 and 4).

Therefore, the Applicant respectfully traverses the Examiner's rejection of Claim 16 and respectfully asserts that Claim 16 is patentable over Flaker et al. Furthermore, Claims 17 – 19 are allowable for depending on allowable independent Claim 16 and, in combination, including limitations not taught or described in the references of record.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,



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